

EX 

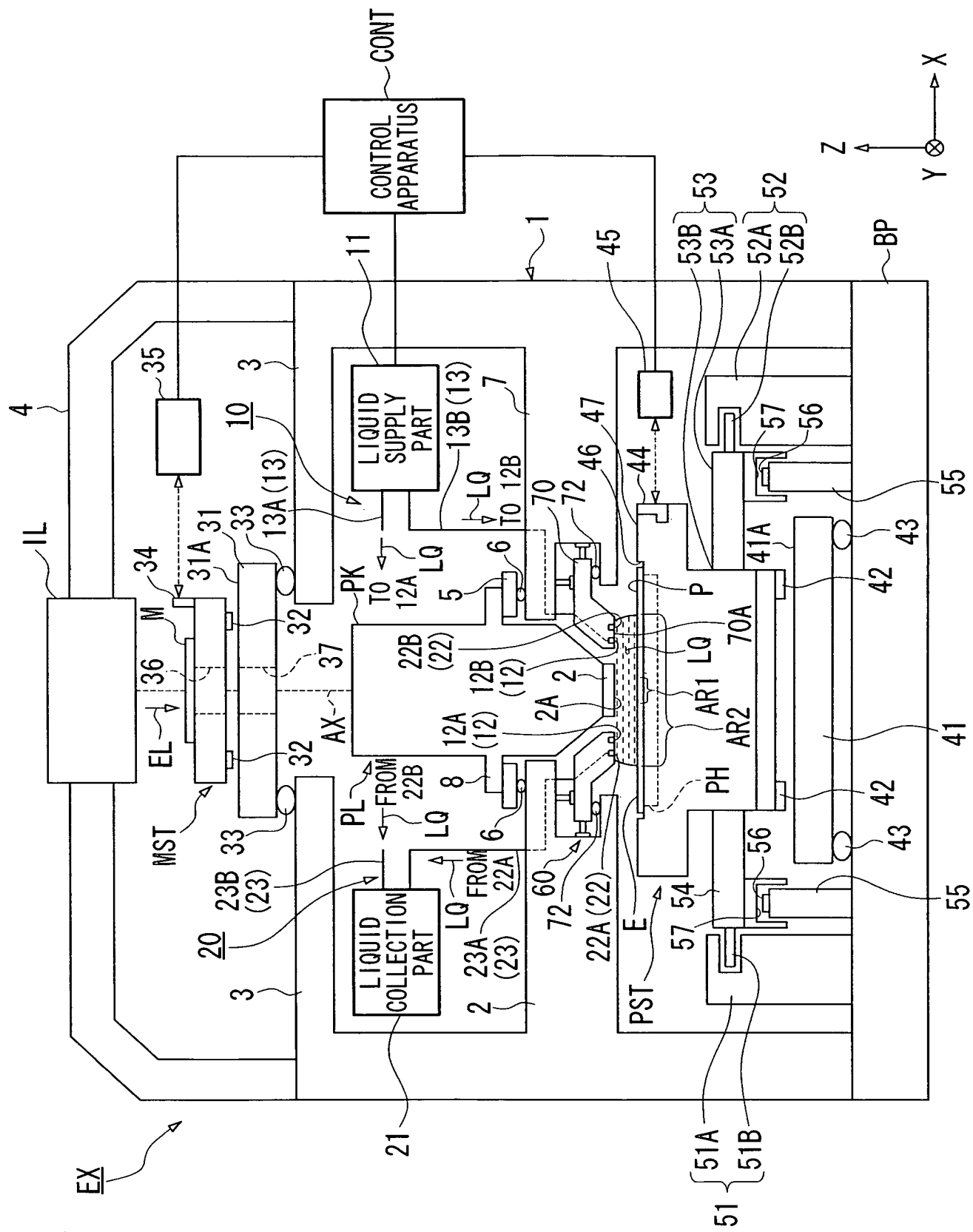


FIG. 2

FIG. 2 is a cross-sectional view of a semiconductor device, specifically a memory array. The device includes a substrate (44) with a passivation layer (46) and a gate stack (47). The gate stack (47) is formed on the substrate (44) and includes a gate dielectric layer (47A) and a gate conductive layer (47B). The gate conductive layer (47B) is patterned to form word lines (70A, 70B) and bit lines (70C, 70D). The word lines (70A, 70B) are formed by a gate stack (70A, 70B) and a gate stack (70A, 70B). The bit lines (70C, 70D) are formed by a gate stack (70C, 70D) and a gate stack (70C, 70D). The storage nodes are formed by a gate stack (70A, 70B) and a gate stack (70A, 70B). The device is labeled with various components: 5, 6, 7(1), 7(2), 7(3), 7(4), 7(5), 7(6), 7(7), 7(8), 7(9), 7(10), 7(11), 7(12), 7(13), 7(14), 7(15), 7(16), 7(17), 7(18), 7(19), 7(20), 7(21), 7(22), 7(23), 7(24), 7(25), 7(26), 7(27), 7(28), 7(29), 7(30), 7(31), 7(32), 7(33), 7(34), 7(35), 7(36), 7(37), 7(38), 7(39), 7(40), 7(41), 7(42), 7(43), 7(44), 7(45), 7(46), 7(47), 7(48), 7(49), 7(50), 7(51), 7(52), 7(53), 7(54), 7(55), 7(56), 7(57), 7(58), 7(59), 7(60), 7(61), 7(62), 7(63), 7(64), 7(65), 7(66), 7(67), 7(68), 7(69), 7(70), 7(71), 7(72), 7(73), 7(74), 7(75), 7(76), 7(77), 7(78), 7(79), 7(80), 7(81), 7(82), 7(83), 7(84), 7(85), 7(86), 7(87), 7(88), 7(89), 7(90), 7(91), 7(92), 7(93), 7(94), 7(95), 7(96), 7(97), 7(98), 7(99), 7(100).

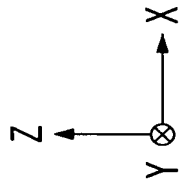


FIG. 3

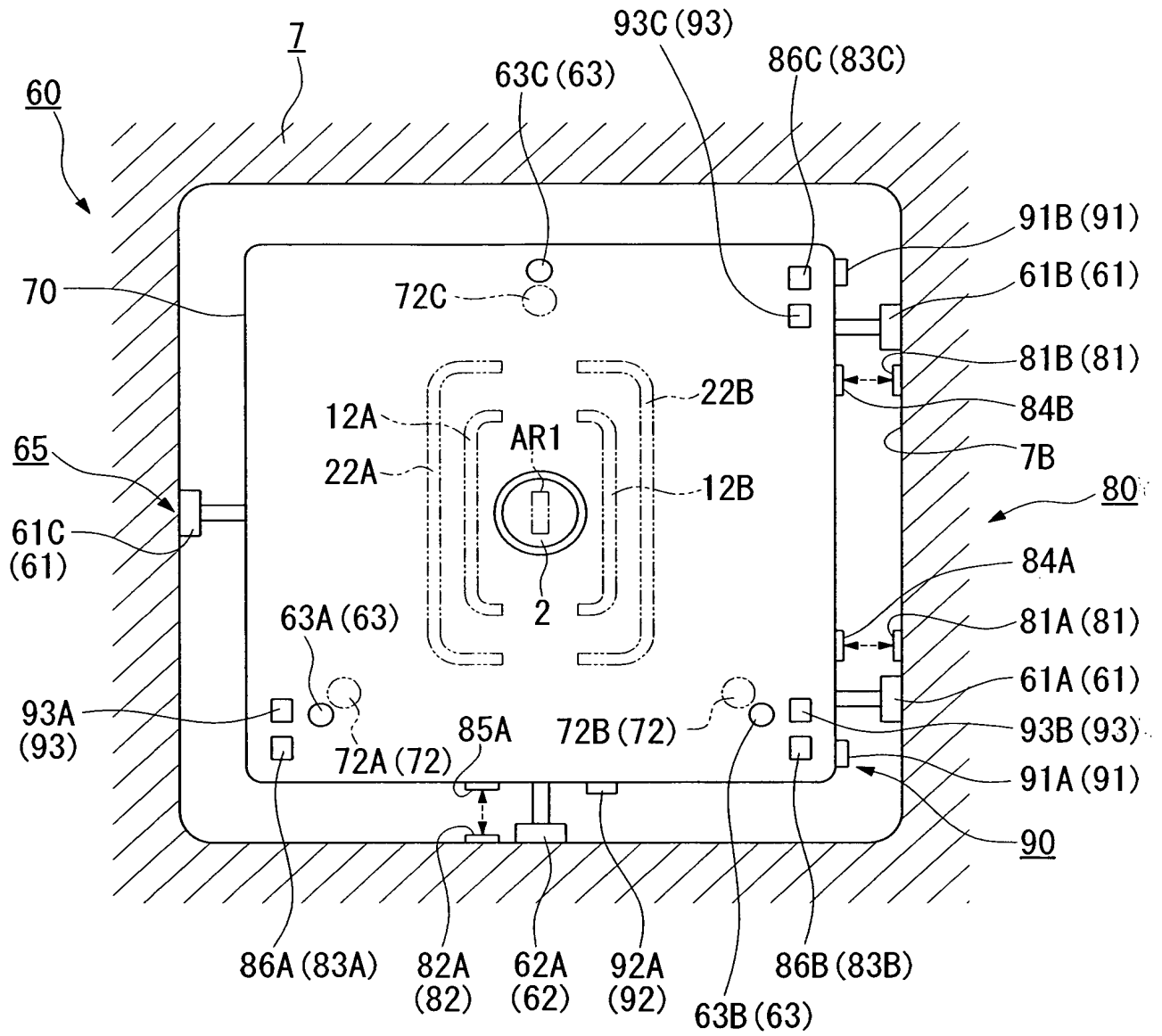


FIG. 4

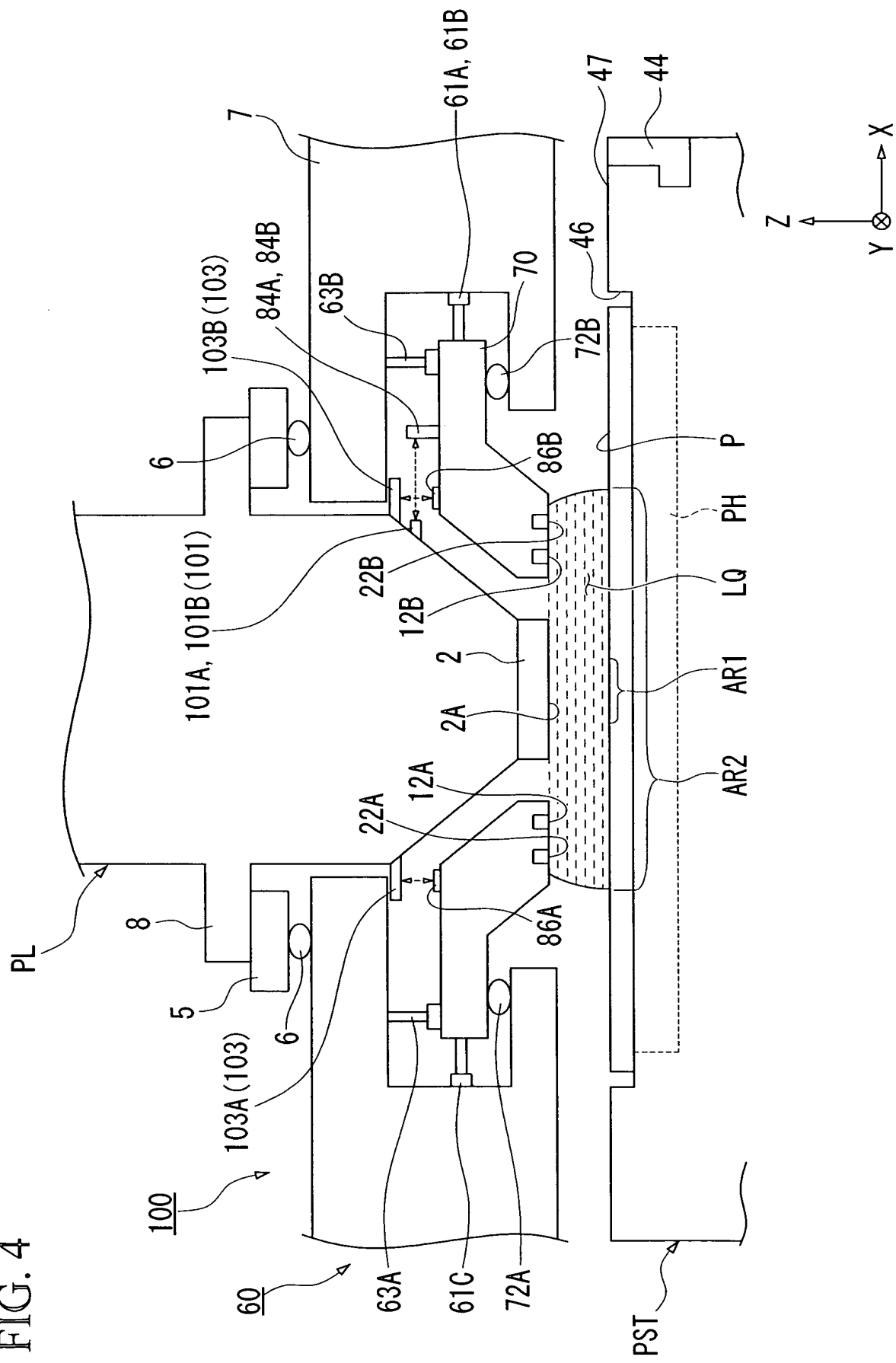


FIG. 5

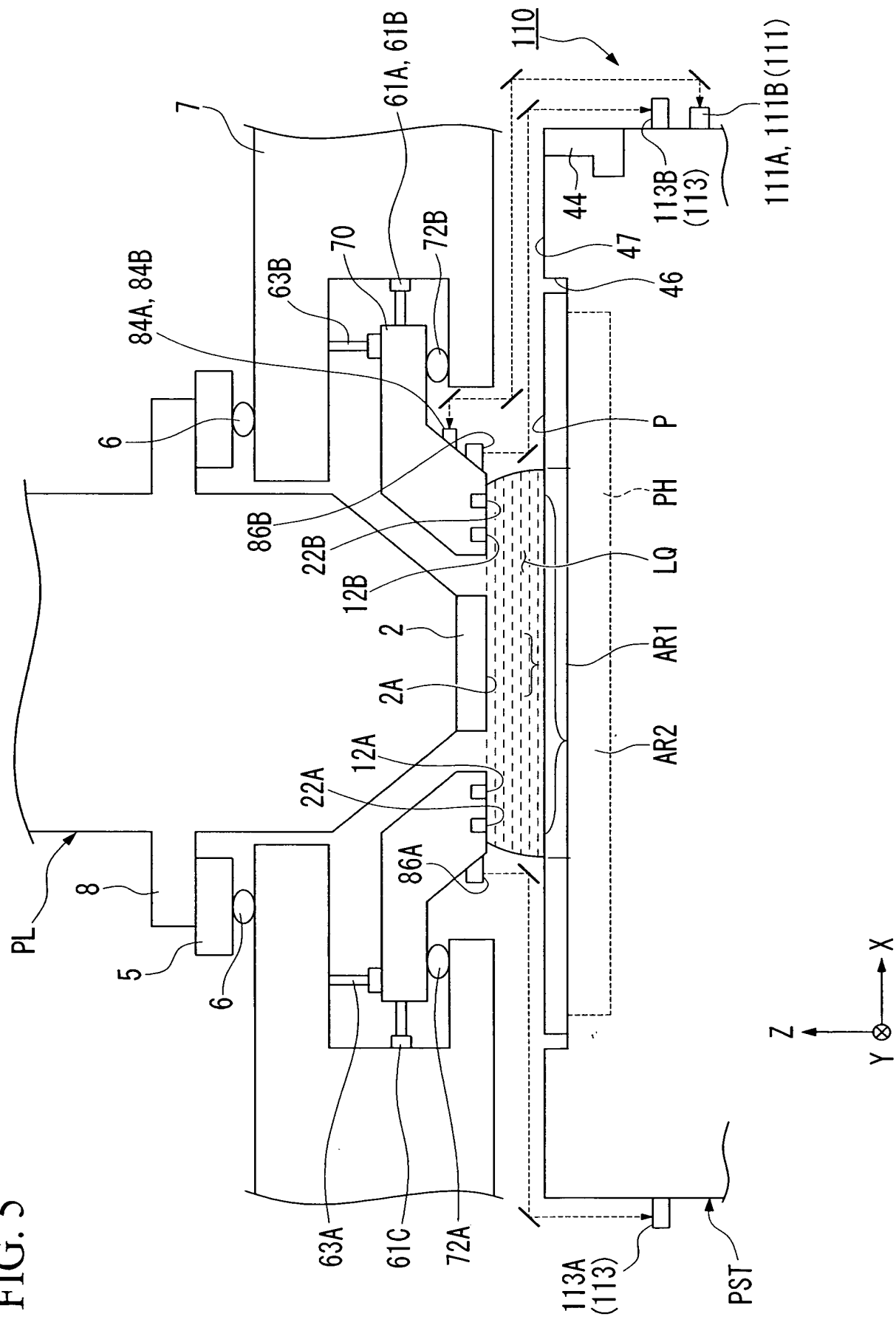


FIG. 6

